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<input type="checkbox"/>	L8	('6744274' '6681354')!.ABPN1,NRPN,PN,TBAN,WKU. <i>DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ</i>	4
<input type="checkbox"/>	L7	((('5878051') [ABPN1,NRPN,PN,TBAN,WKU]) and @pd > 20040113 (L5 and (test\$3 or inspect\$4 or check\$4 or debug\$4 or verif\$7 or diagno\$5 or probing or probe or exerci\$4 or stimul\$7) near2 (self\$3 or built\$4) same (pld or spld or cpld or fpga or programmable near2 (logic or device)) same configur\$7 same (rom or prom or eeprom or read\$1only near memory)) and @pd > 20040113	0
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<input type="checkbox"/>	L5	((test\$3 or inspect\$4 or check\$4 or debug\$4 or verif\$7 or diagno\$5 or probing or probe or exerci\$4 or stimul\$7) near2 (self\$3 or built\$4) same (pld or spld or cpld or fpga or programmable near2 (logic or device)) same configur\$7) and @pd > 20040113 <i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>	16
<input type="checkbox"/>	L4	('6574761')!.PN.	2
<input type="checkbox"/>	L3	(fpga with (self\$1 or built\$4) near2 test\$3 same logic\$4 and fpga with (self\$1 or built\$4) near2 test\$3)	40
<input type="checkbox"/>	L2	(fpga with (self\$1 or built\$4) near2 test\$3)	75
<input type="checkbox"/>	L1	(fpga with (self\$1 or built\$4) near2 test\$3 same logic\$4 and format and fpga with (self\$1 or built\$4) near2 test\$3 same logic\$4 and fpga with (self\$1 or built\$4) near2 test\$3)	6

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## 1 Design of self-testing checkers for Borden codes

*Piestrak, S.J.;*

Computers, IEEE Transactions on , Volume: 45 , Issue: 4 , April 1996

Pages:461 - 469

[Abstract] [PDF Full-Text (828 KB)] **IEEE JNL**

## 2 A 16ns CMOS EEPLA with reprogrammable architecture

*Rutledge, D.; Turner, J.; Darling, R.; Josephson, G.;*

Solid-State Circuits Conference. Digest of Technical Papers. 1986  
IEEE International , Volume: XXIX , Feb 1986

Pages:240 - 241

[Abstract] [PDF Full-Text (880 KB)] **IEEE CNF**

## 3 A 32-bit microprocessor with efficient testable designs, the TX2

*Nozuyama, Y.; Mitani, H.; Fukumoto, T.; Utsumi, T.; Hashimoto, K.;*

TRON Project International Symposium, 1994., Proceedings of the 11th , 7-10 Dec. 1994

Pages:122 - 130

[Abstract] [PDF Full-Text (472 KB)] **IEEE CNF**

## 4 A hardware approach to self-testing of large programmable logic arrays

*Daehn, W.; Mucha, J.;*

Circuits and Systems, IEEE Transactions on , Volume: 28 , Issue: 11 , Nov 1981

Pages:1033 - 1037

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[\[Abstract\]](#) [\[PDF Full-Text \(504 KB\)\]](#) **IEEE JNL**

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**5 Enhancement of Australian VHF combat net radios**

*Weimin Zhang; Rice, M.;*

Military Communications Conference, 2001. MILCOM 2001.

Communications for Network-Centric Operations: Creating the Information Force. IEEE , Volume: 1 , 28-31 Oct. 2001

Pages:185 - 189 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(91 KB\)\]](#) **IEEE CNF**

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**6 Implementing a self-testing 8051 microprocessor**

*Cota, E.F.; Krug, M.R.; Lubaszewski, M.; Carro, L.; Susin, A.A.;*

Integrated Circuits and Systems Design, 1999. Proceedings. XII Symposium on , 29 Sept.-2 Oct. 1999

Pages:202 - 205

[\[Abstract\]](#) [\[PDF Full-Text \(24 KB\)\]](#) **IEEE CNF**

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**7 TEXAS: a testing methodology guided by AI techniques**

*Cosgrove, S.J.; Burgess, N.; Musgrave, G.;*

Design for Testability, IEE Colloquium on , 3 Mar 1988

Pages:8/1 - 8/8

[\[Abstract\]](#) [\[PDF Full-Text \(276 KB\)\]](#) **IEE CNF**

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